

FIG. 1A (RELATED ART)

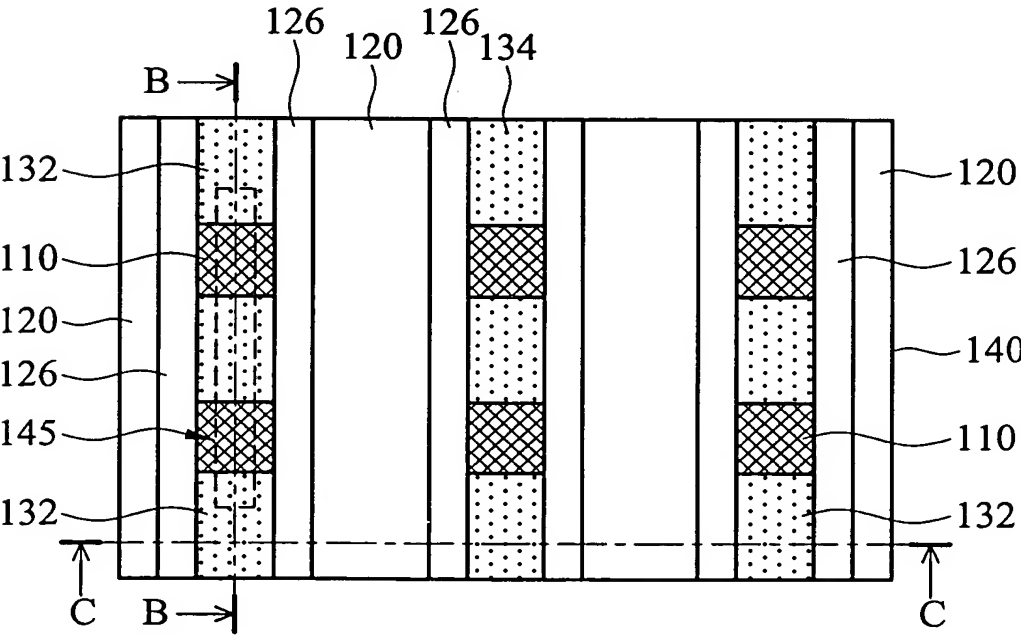


FIG. 1B (RELATED ART)

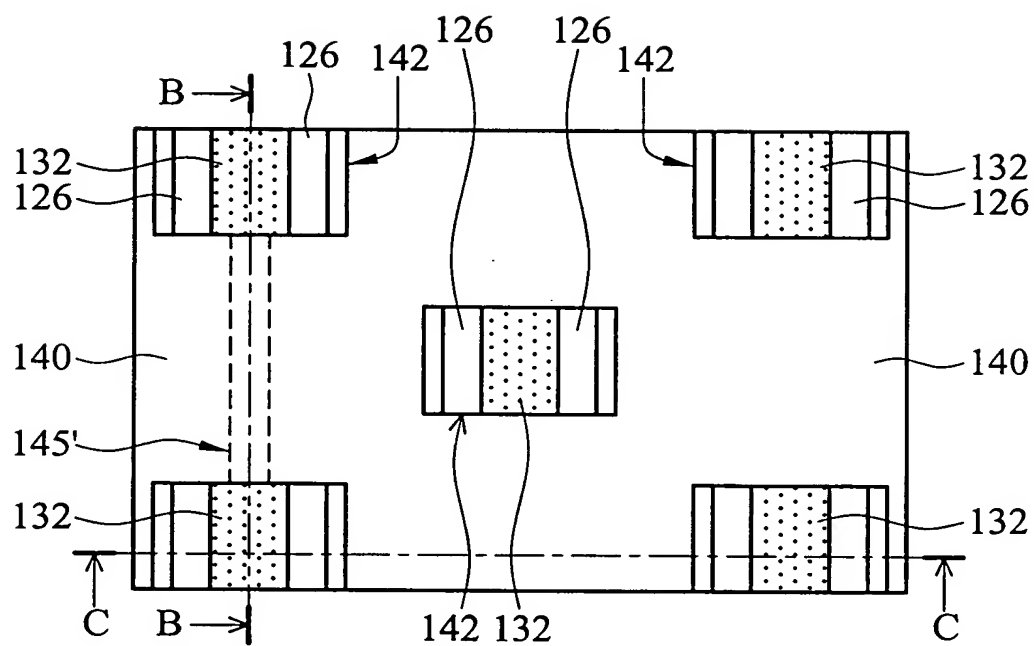


FIG. 1C (RELATED ART)

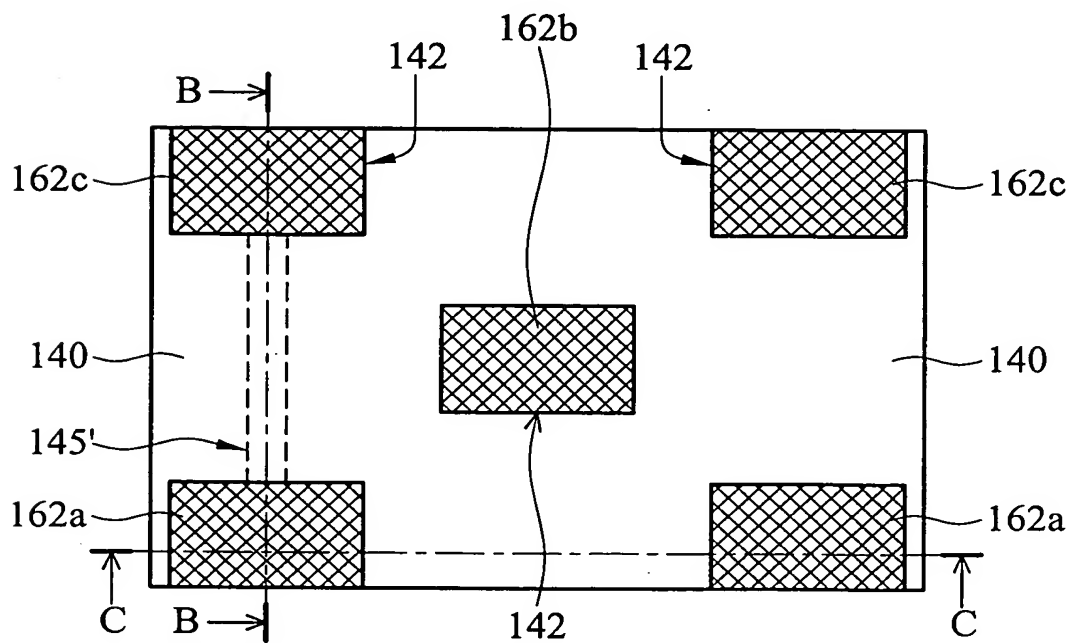


FIG. 1D (RELATED ART)

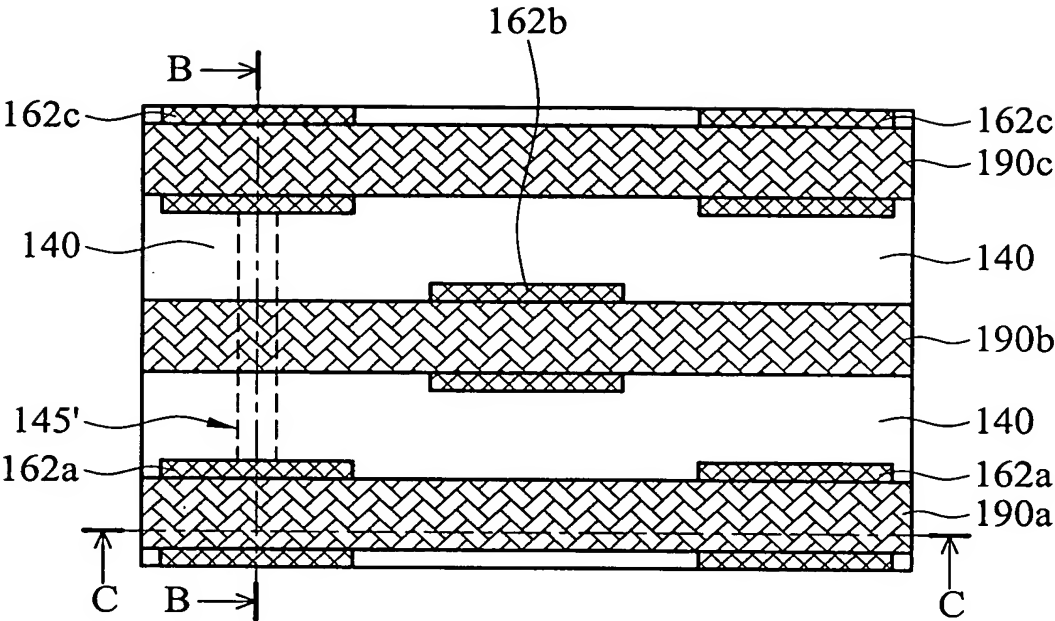


FIG. 1E (RELATED ART)

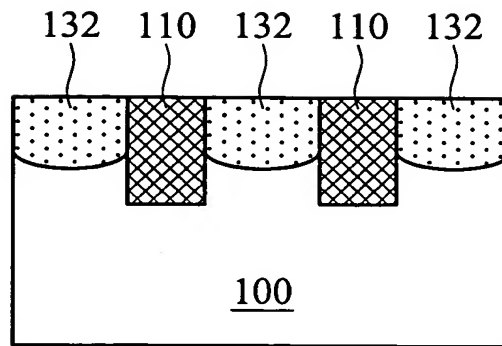


FIG. 2A (RELATED ART)

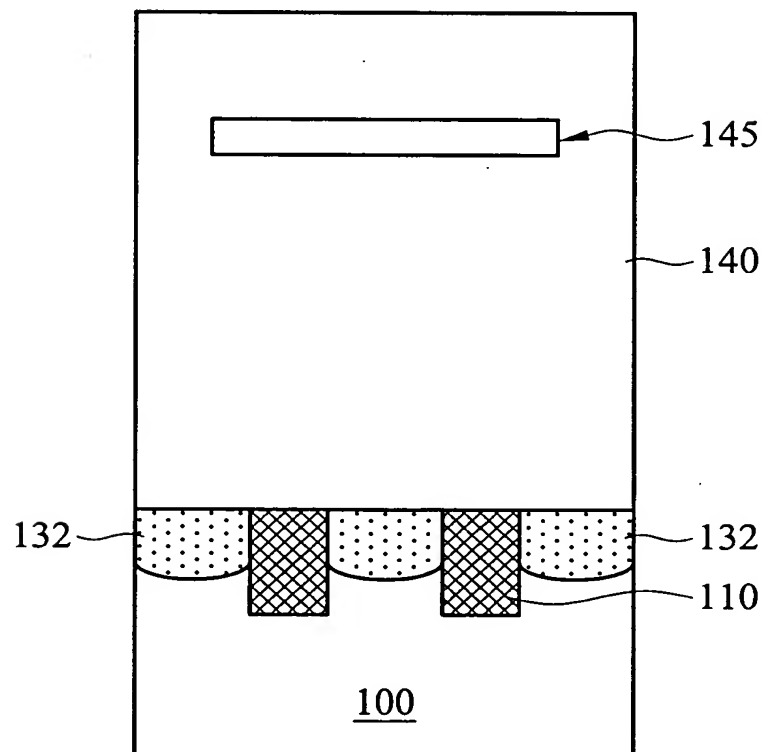


FIG. 2B (RELATED ART)

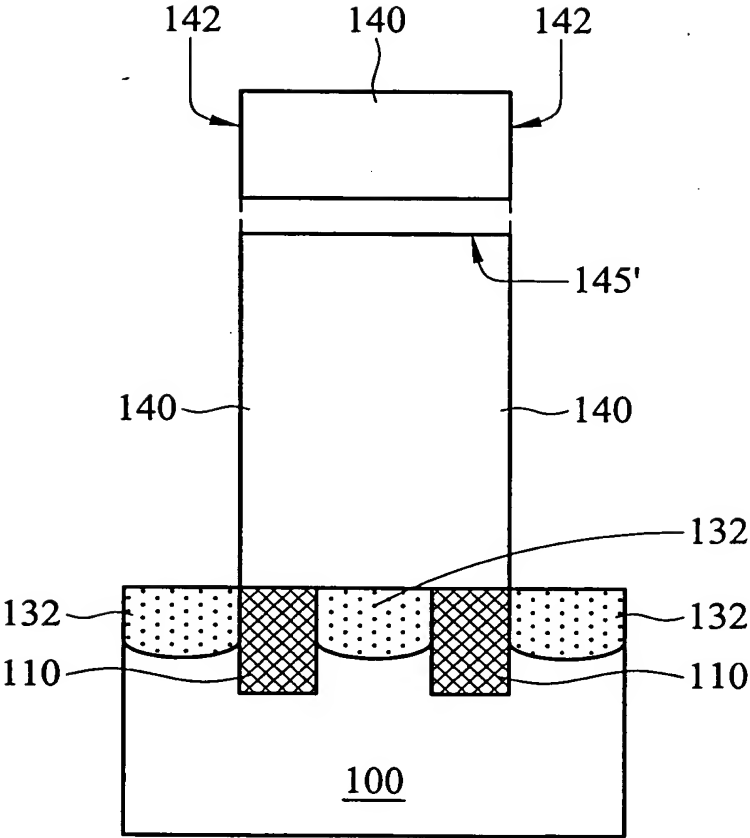


FIG. 2C (RELATED ART)

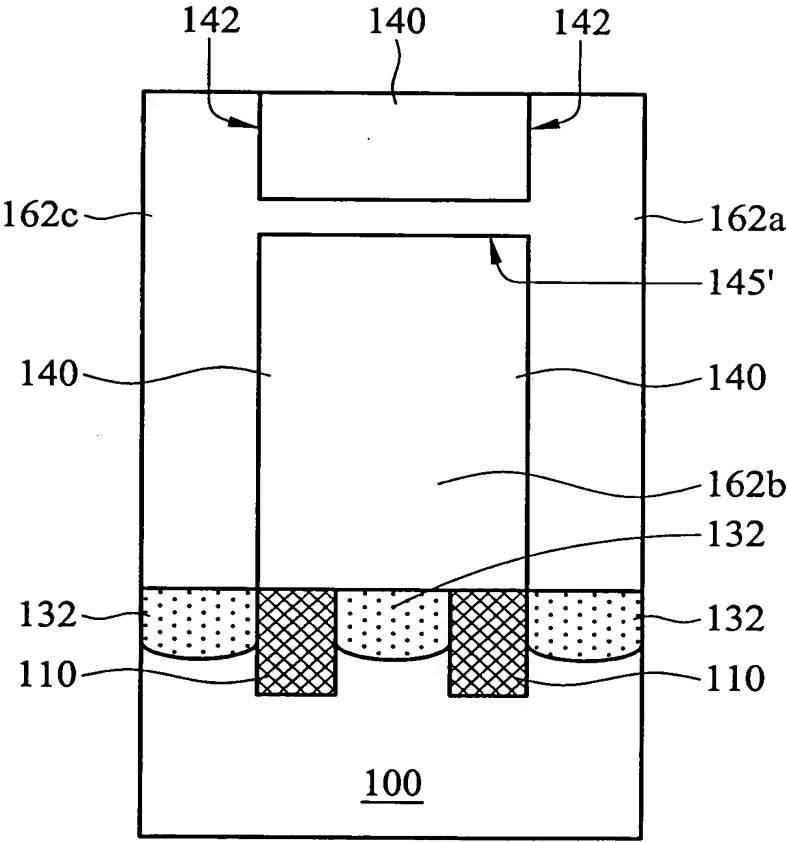


FIG. 2D (RELATED ART)

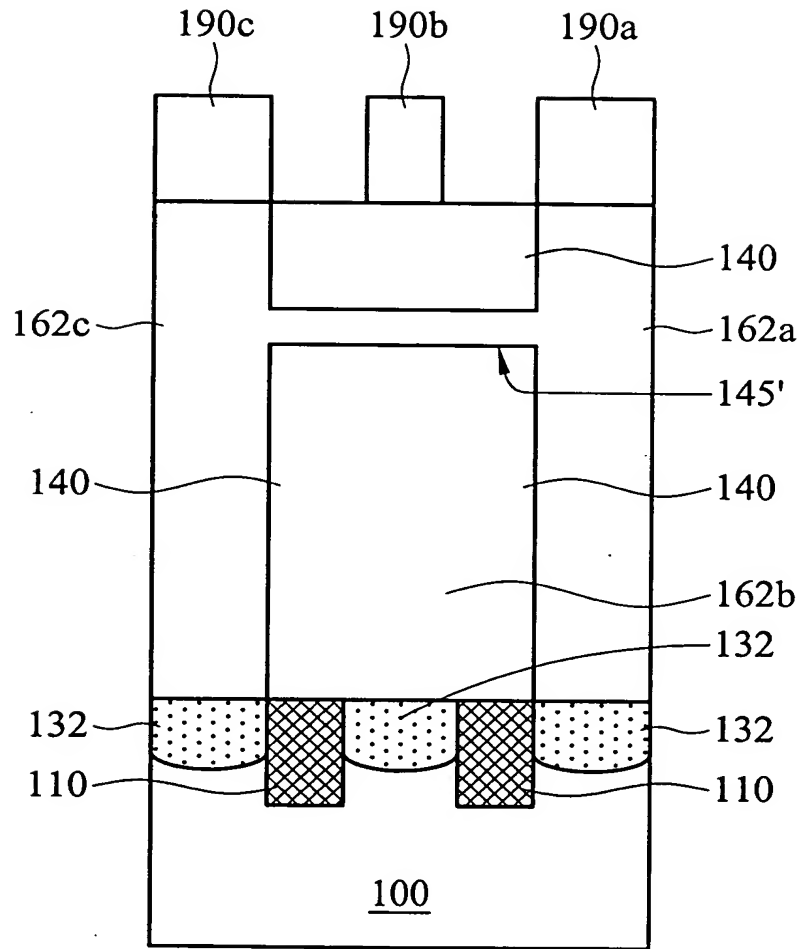


FIG. 2E (RELATED ART)

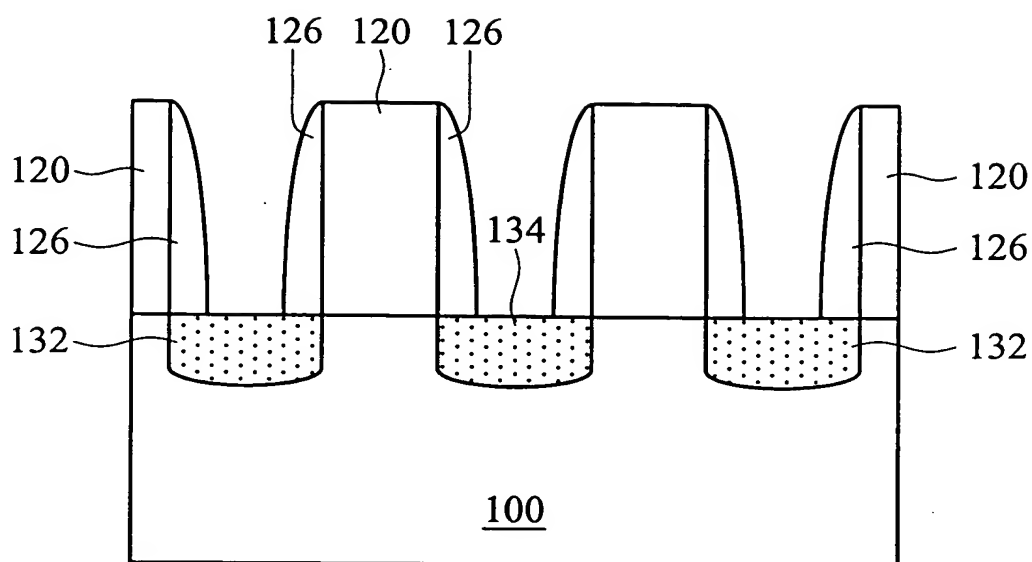


FIG. 3A (RELATED ART)

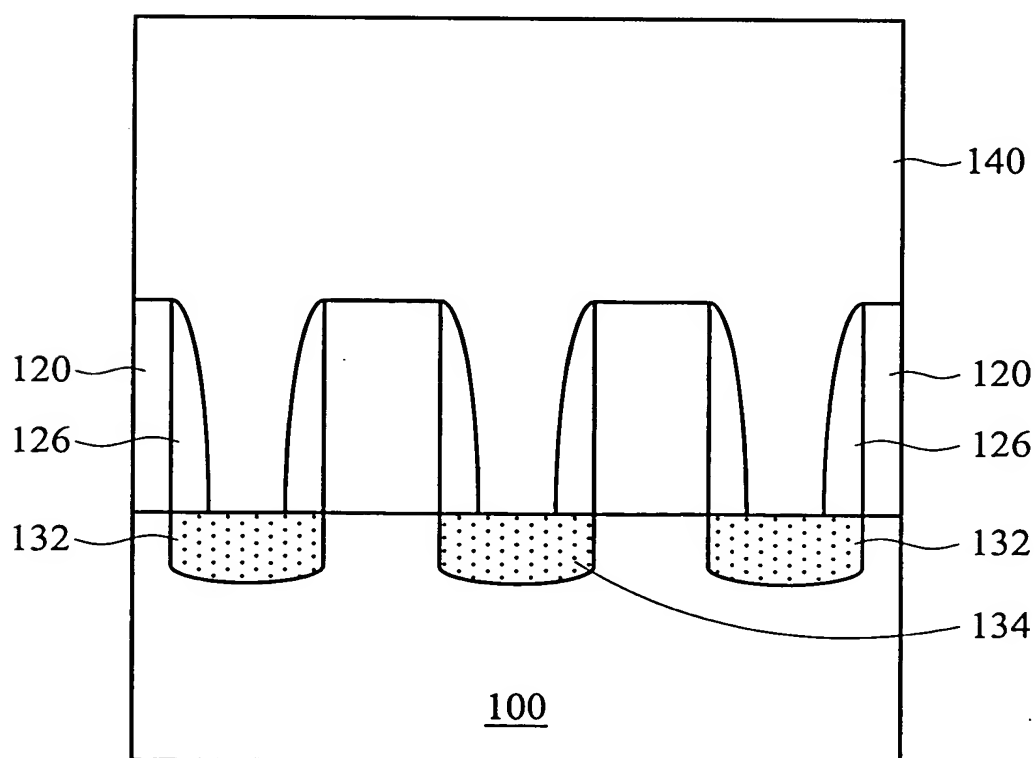


FIG. 3B (RELATED ART)



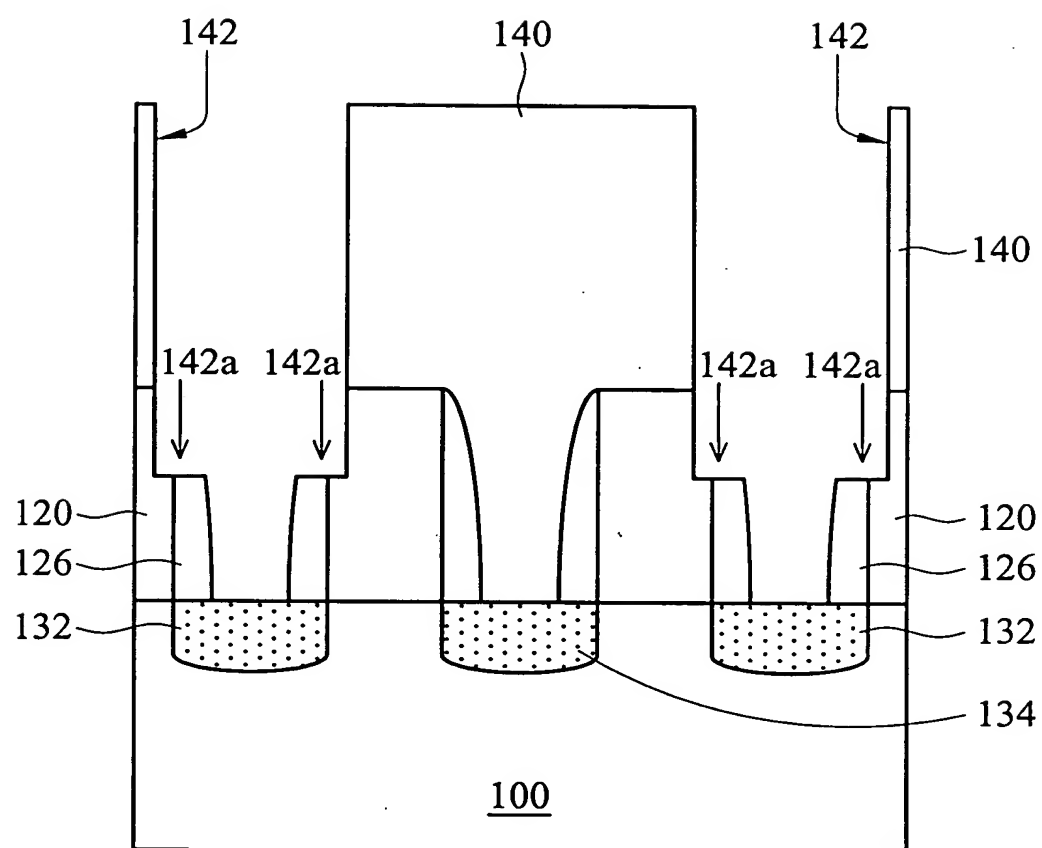


FIG. 3C (RELATED ART)

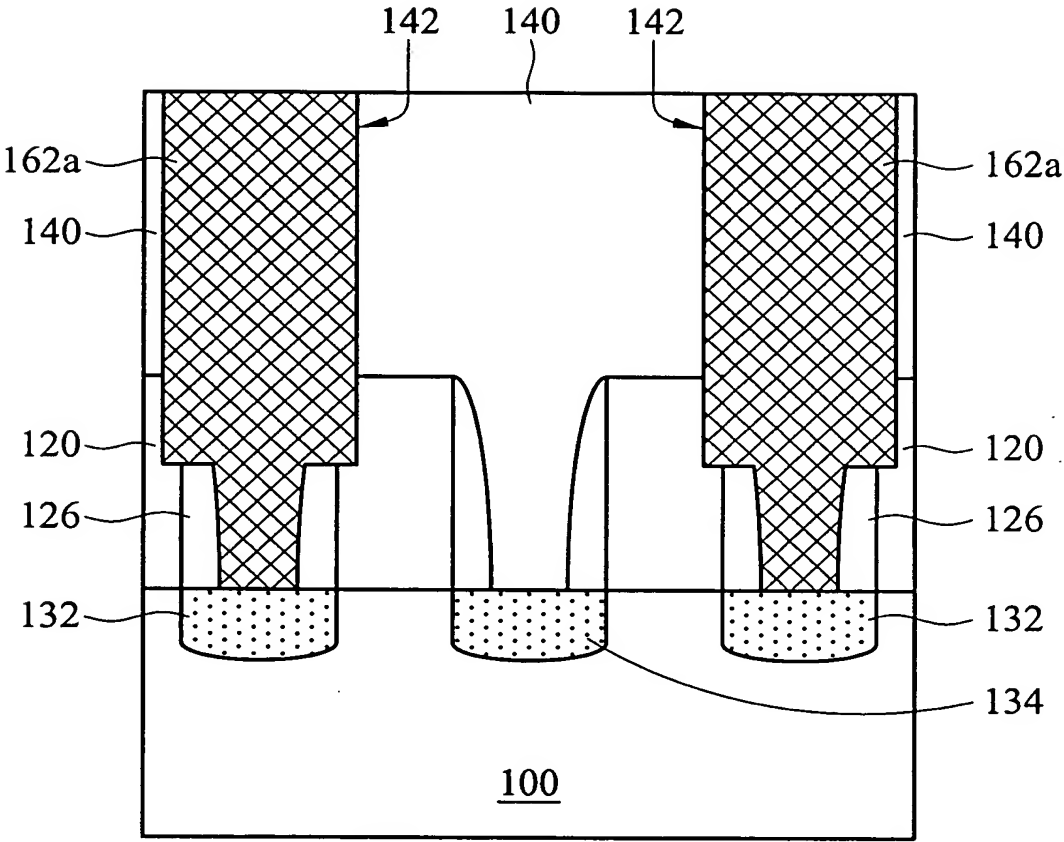


FIG. 3D (RELATED ART)

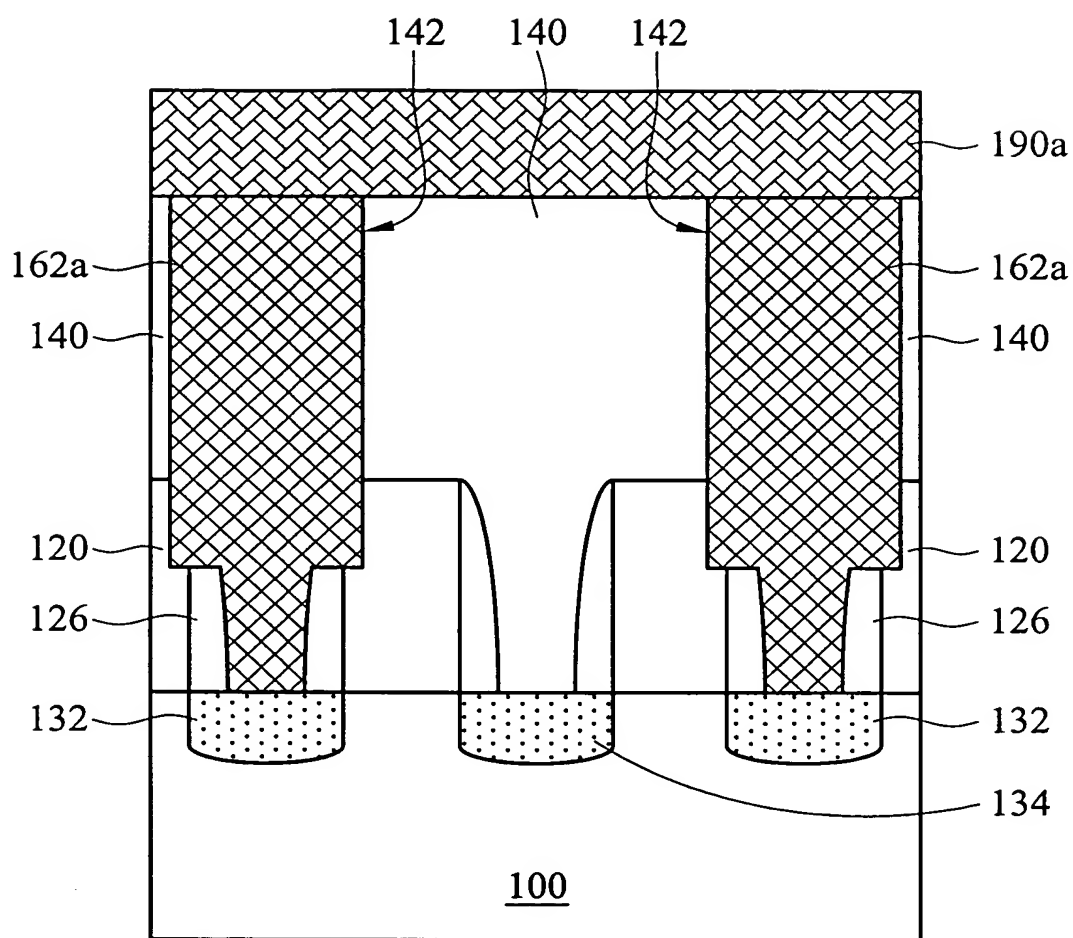


FIG. 3E (RELATED ART)

A cross-sectional view of a semiconductor device. The device consists of a central region 220 flanked by two identical structures. Each side structure includes a bottom layer 232, a layer 226, a layer 240a, a layer 210, and a top layer 232. The top layer 232 is further divided into a dotted region 234 and a cross-hatched region 226. A dashed line is shown at the bottom of the central region 220. Labels B and C with arrows indicate specific dimensions or regions.

FIG. 4B

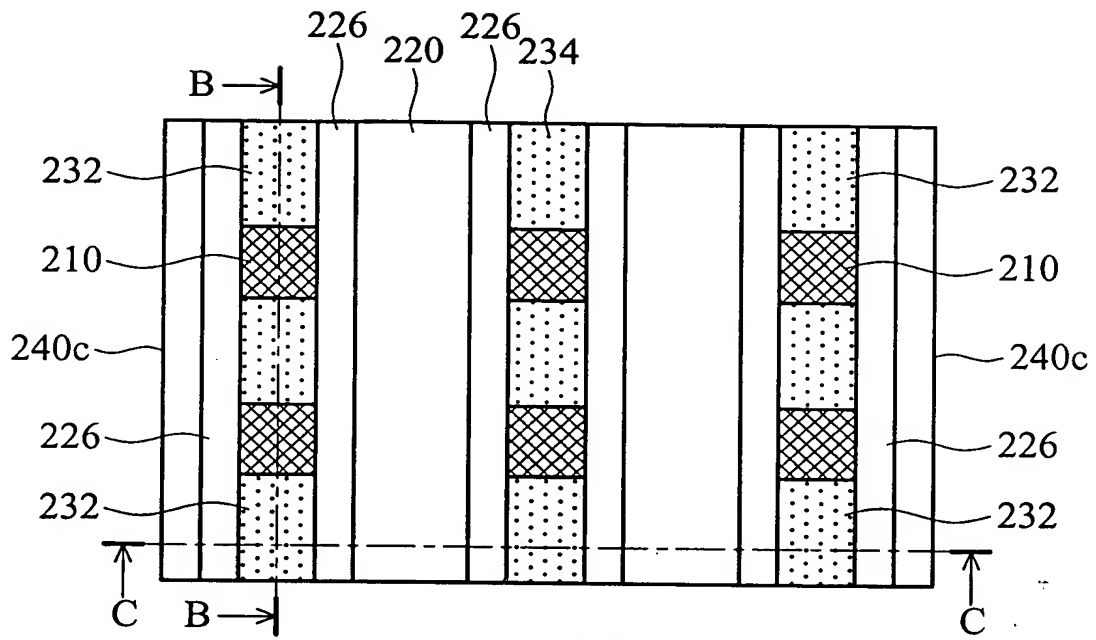


FIG. 4C

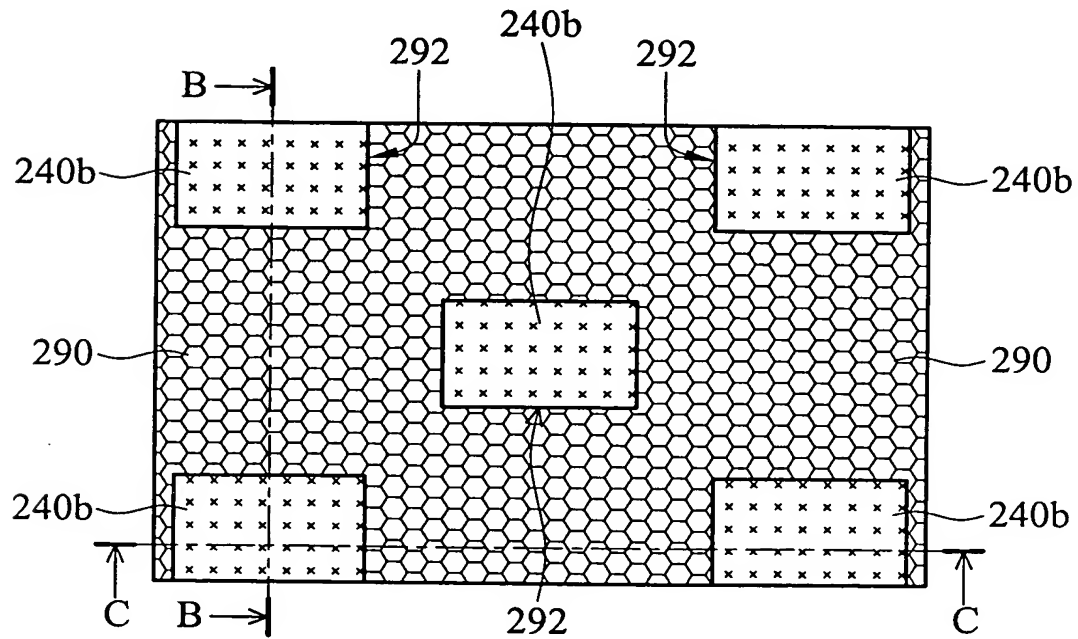


FIG. 4D

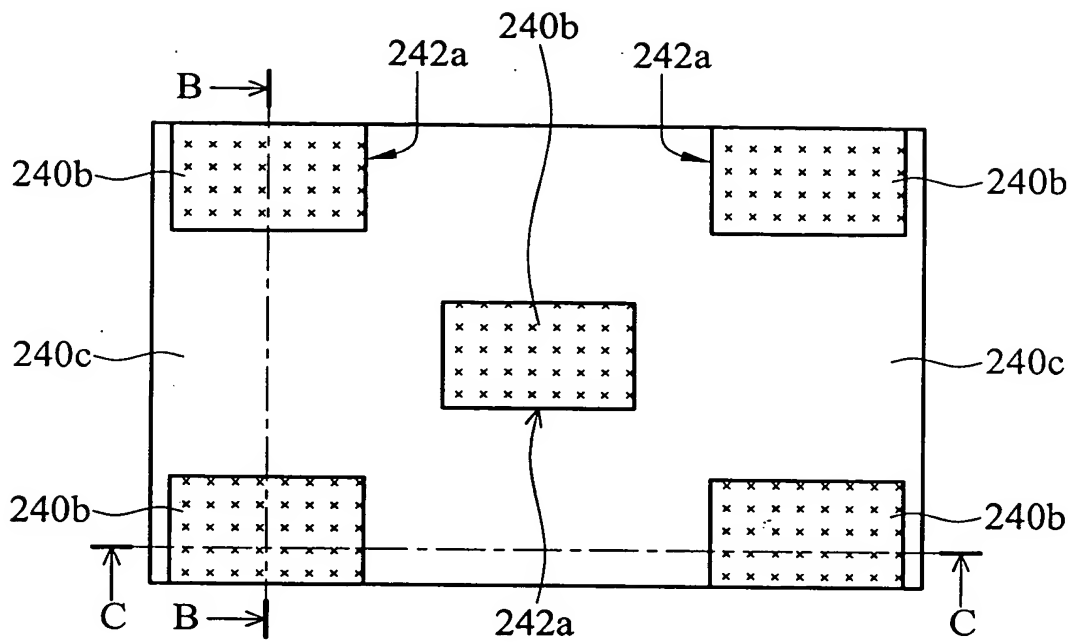


FIG. 4E

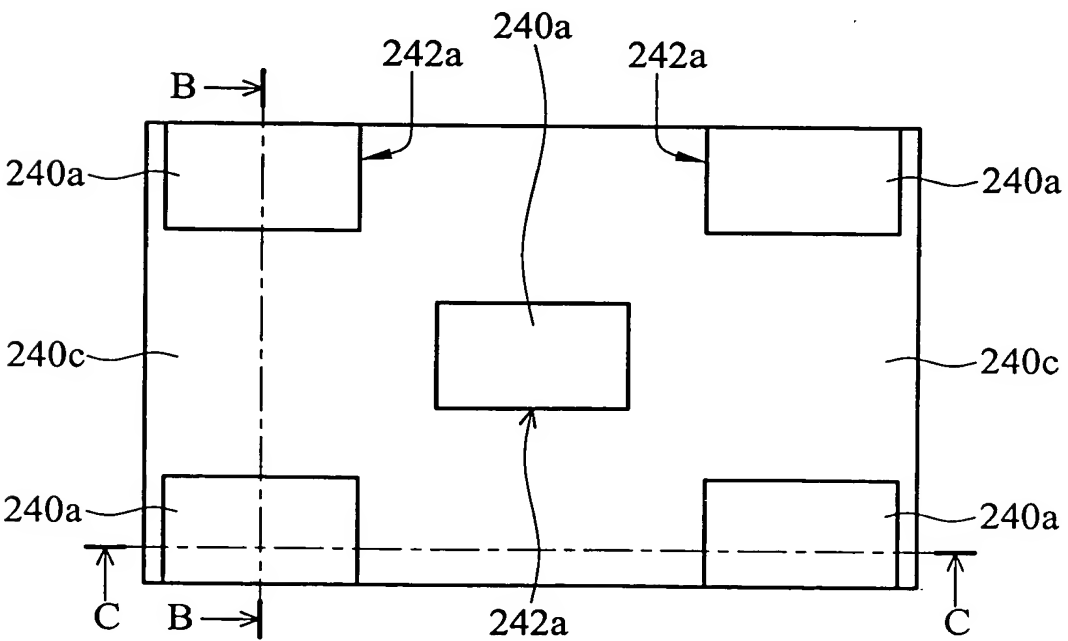


FIG. 4F

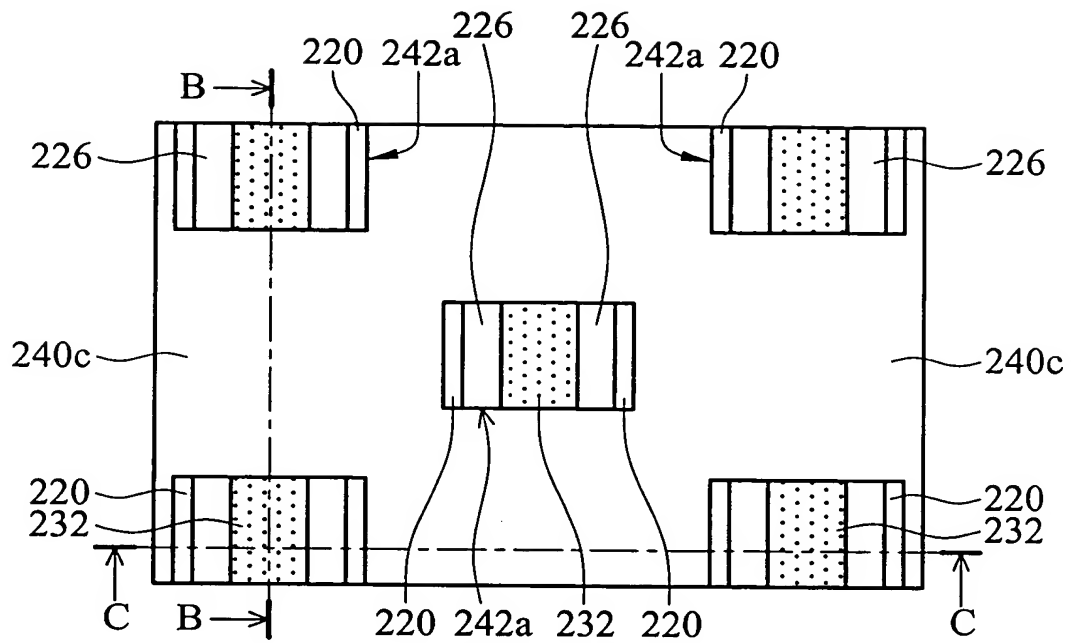


FIG. 4G

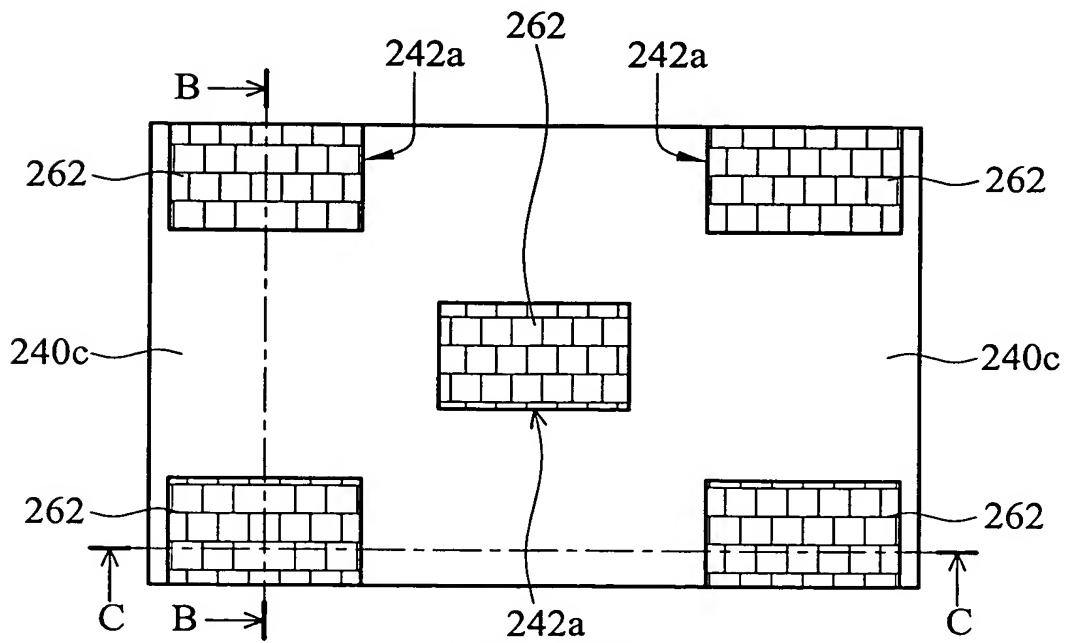


FIG. 4H

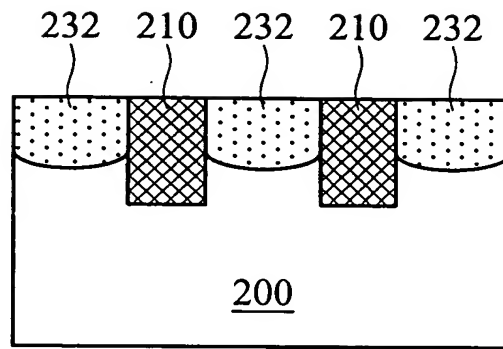


FIG. 5A

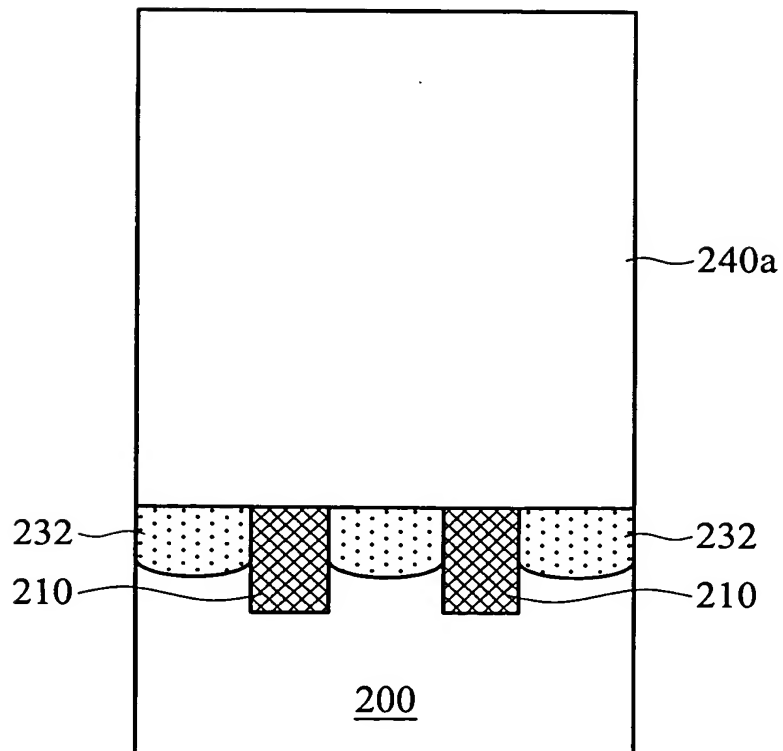


FIG. 5B



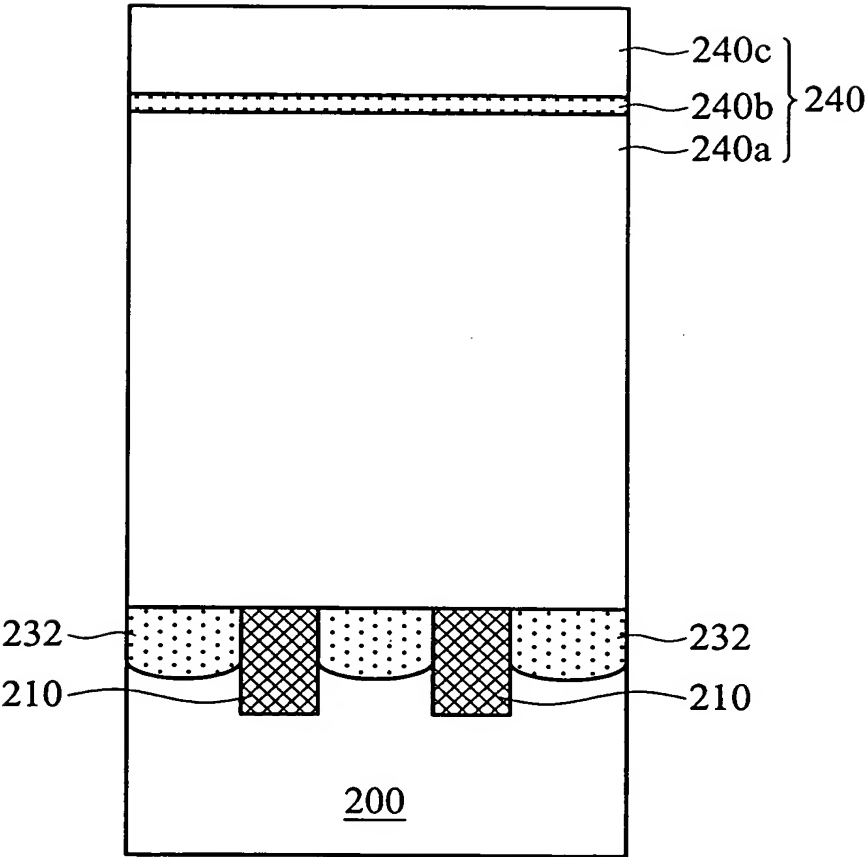


FIG. 5C

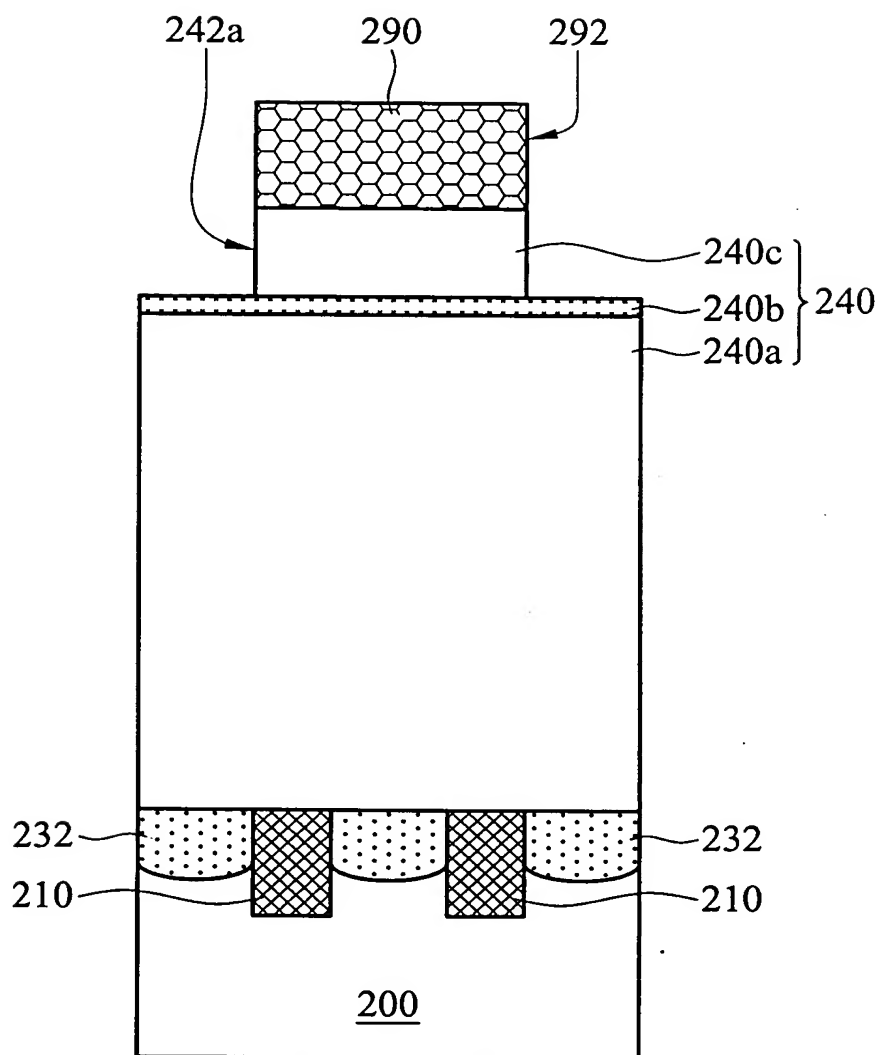


FIG. 5D

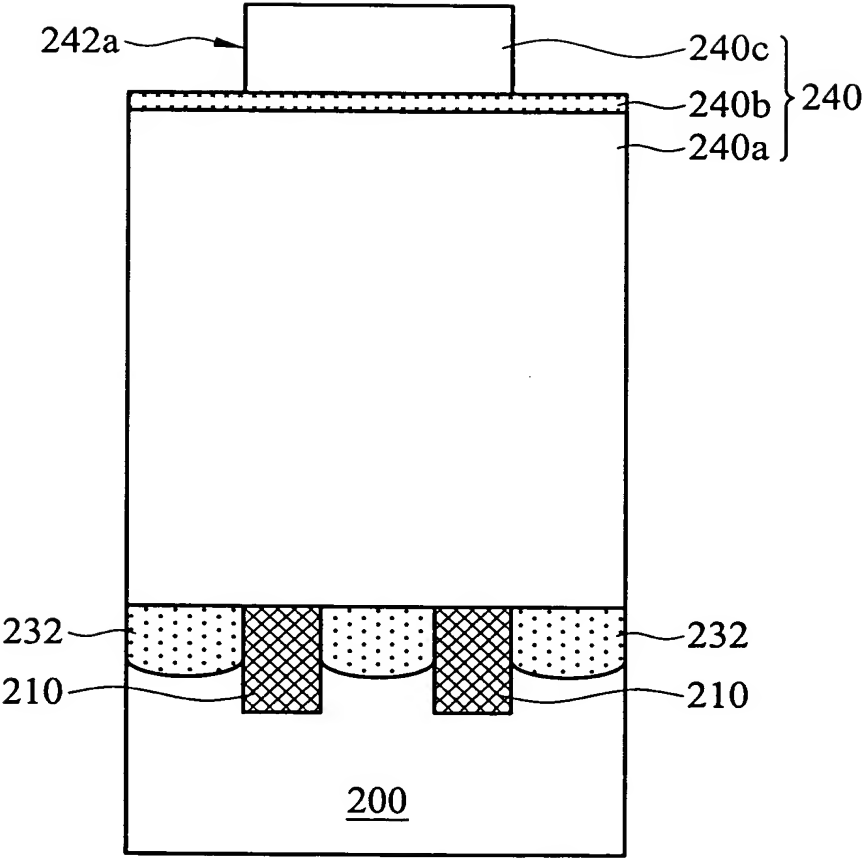


FIG. 5E

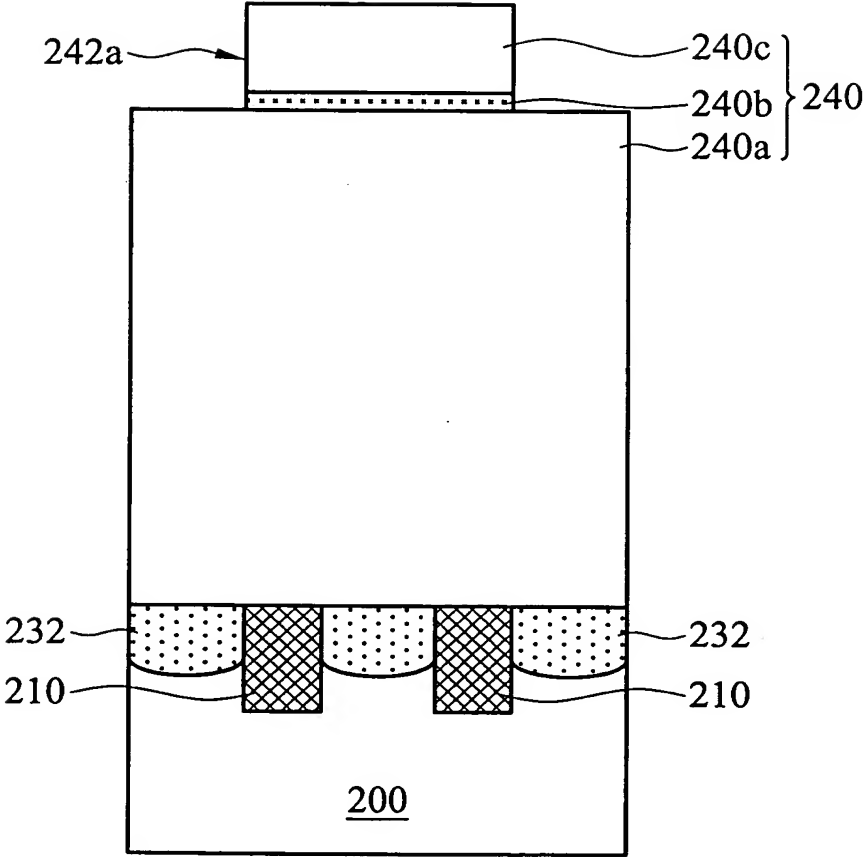


FIG. 5F

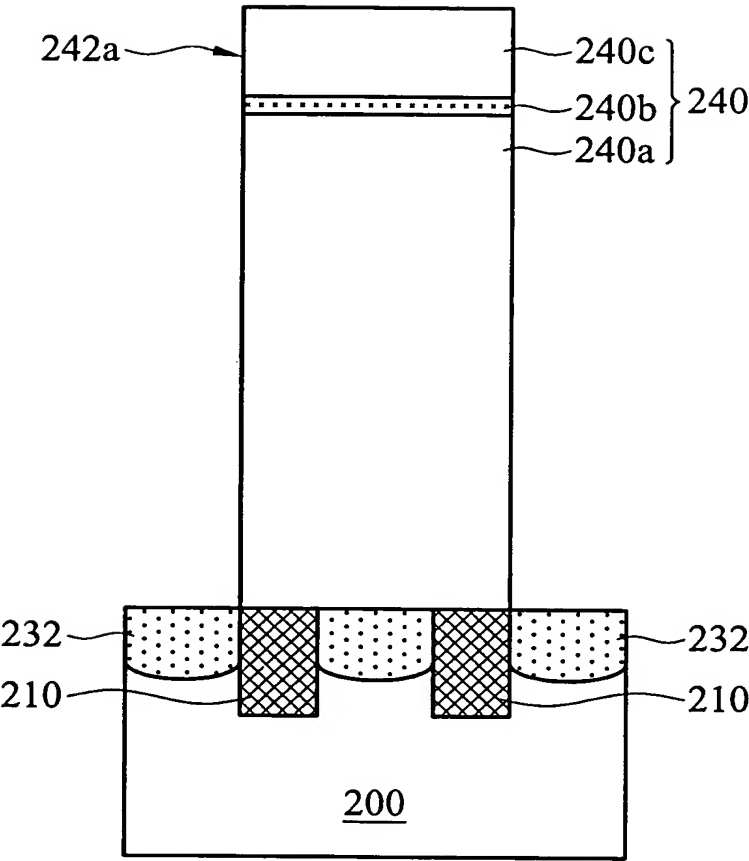


FIG. 5G

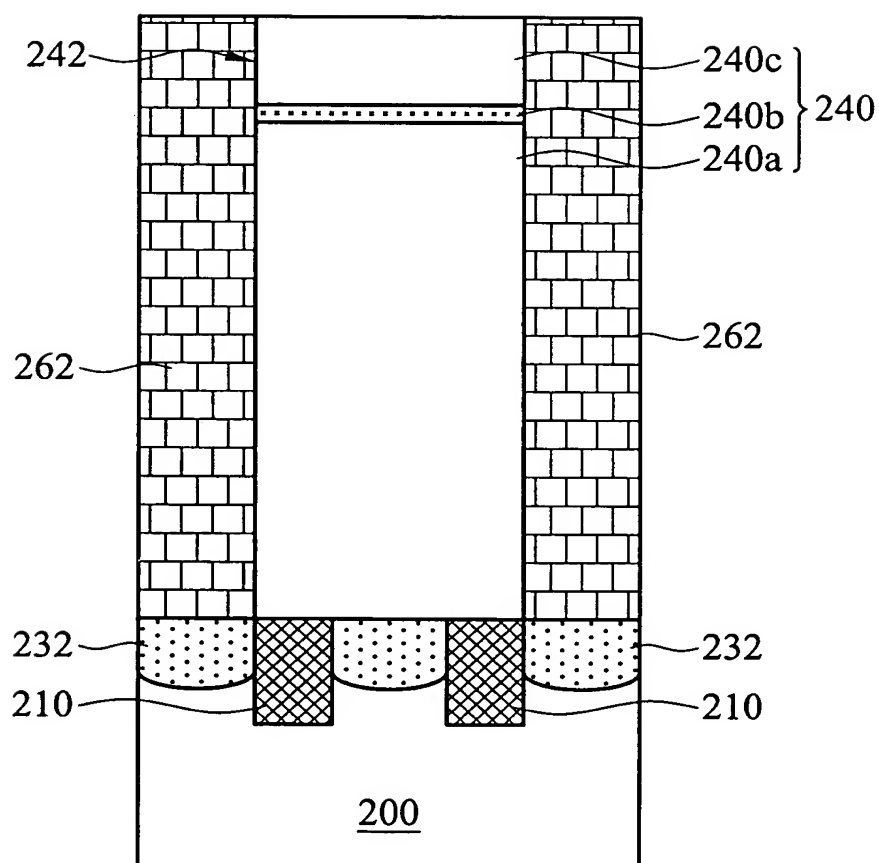


FIG. 5H

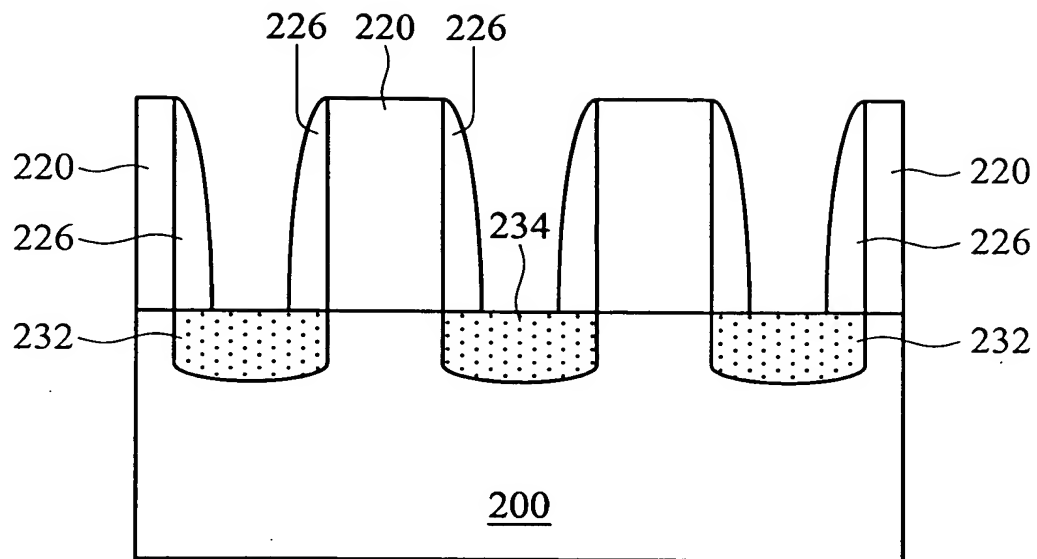


FIG. 6A

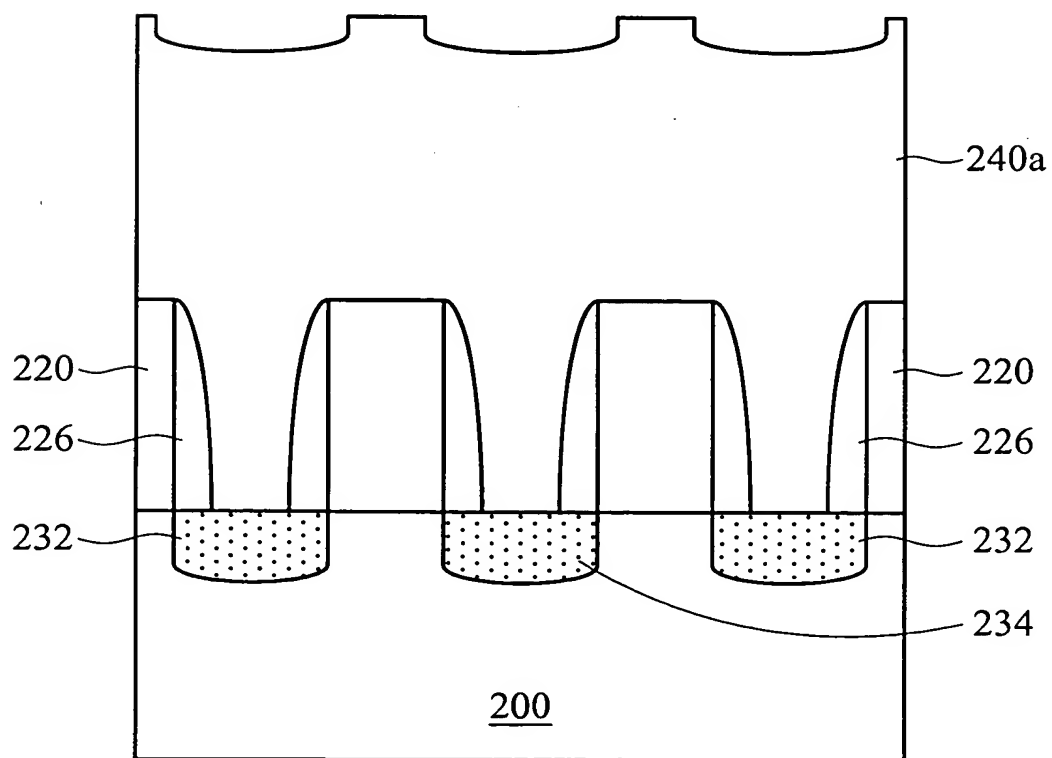


FIG. 6B

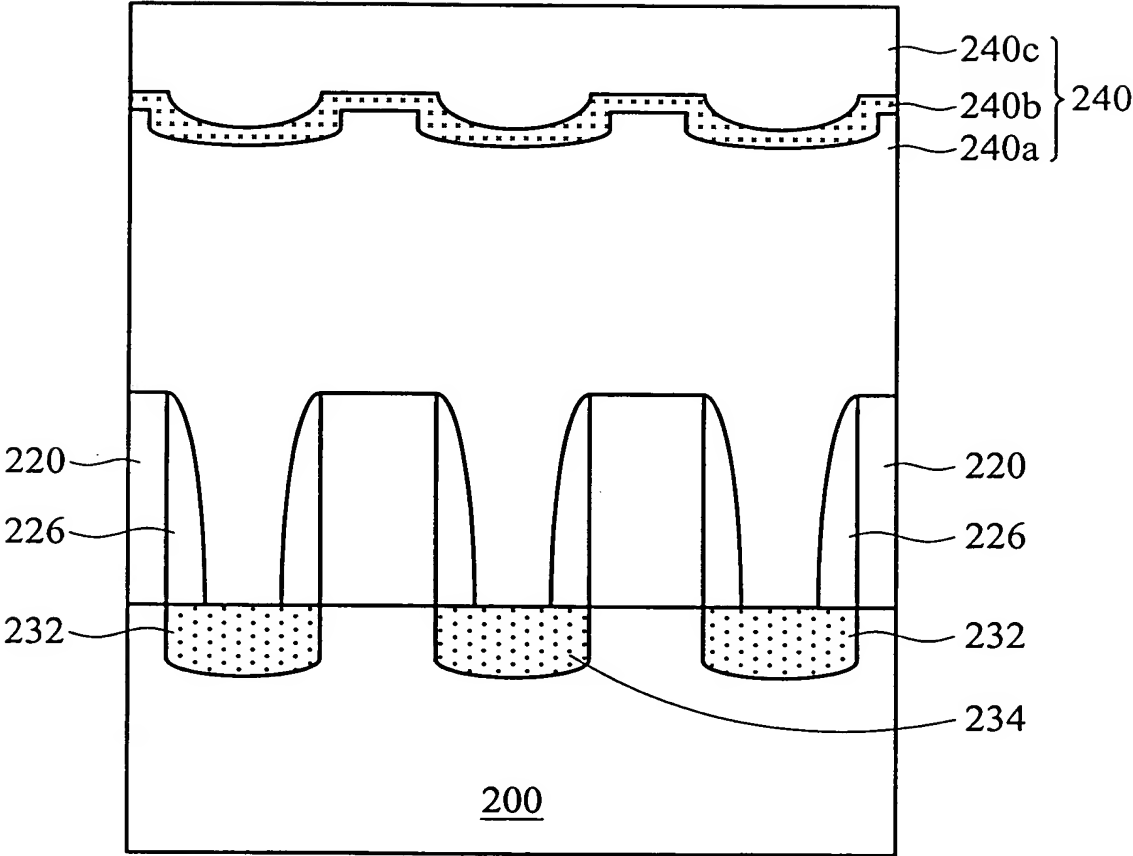


FIG. 6C



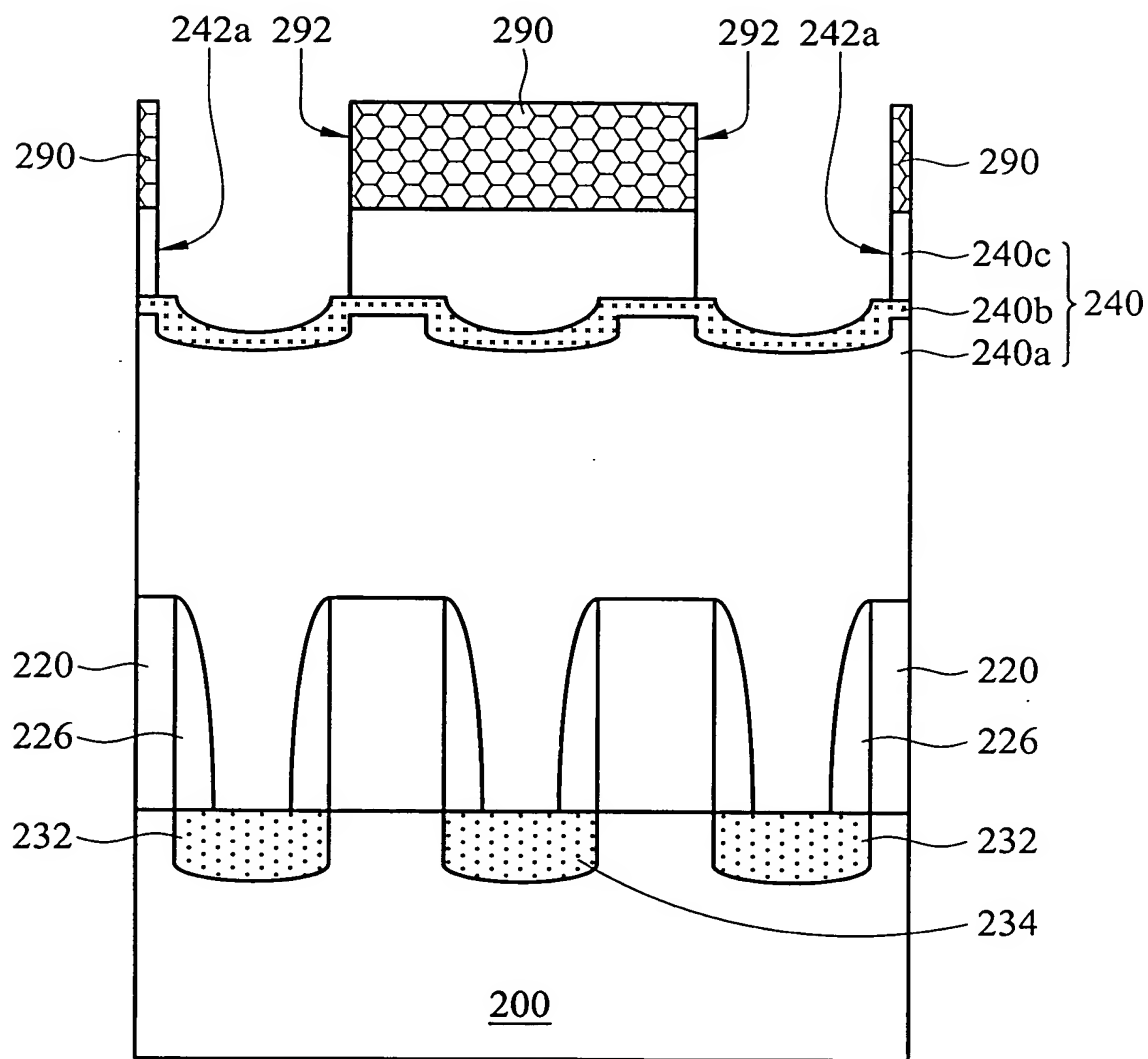


FIG. 6D

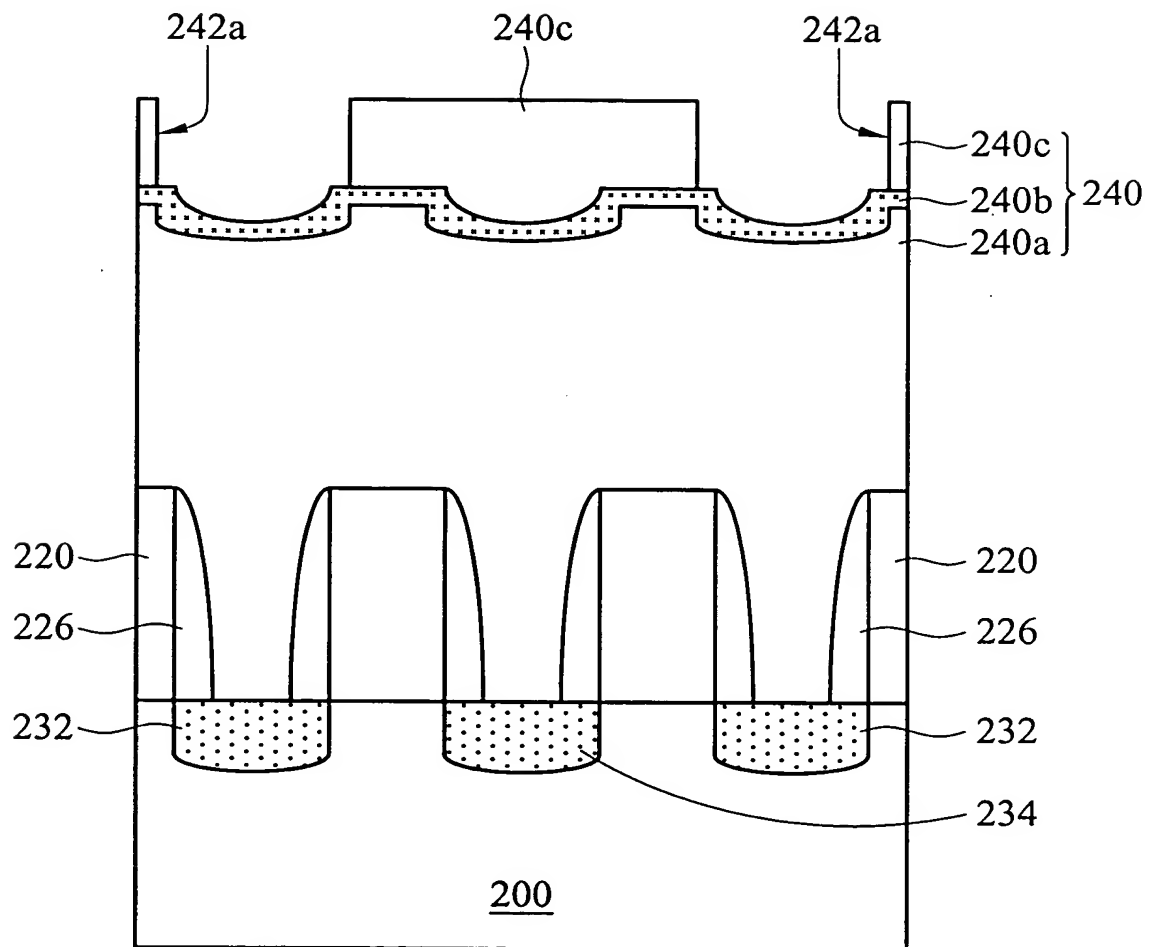


FIG. 6E

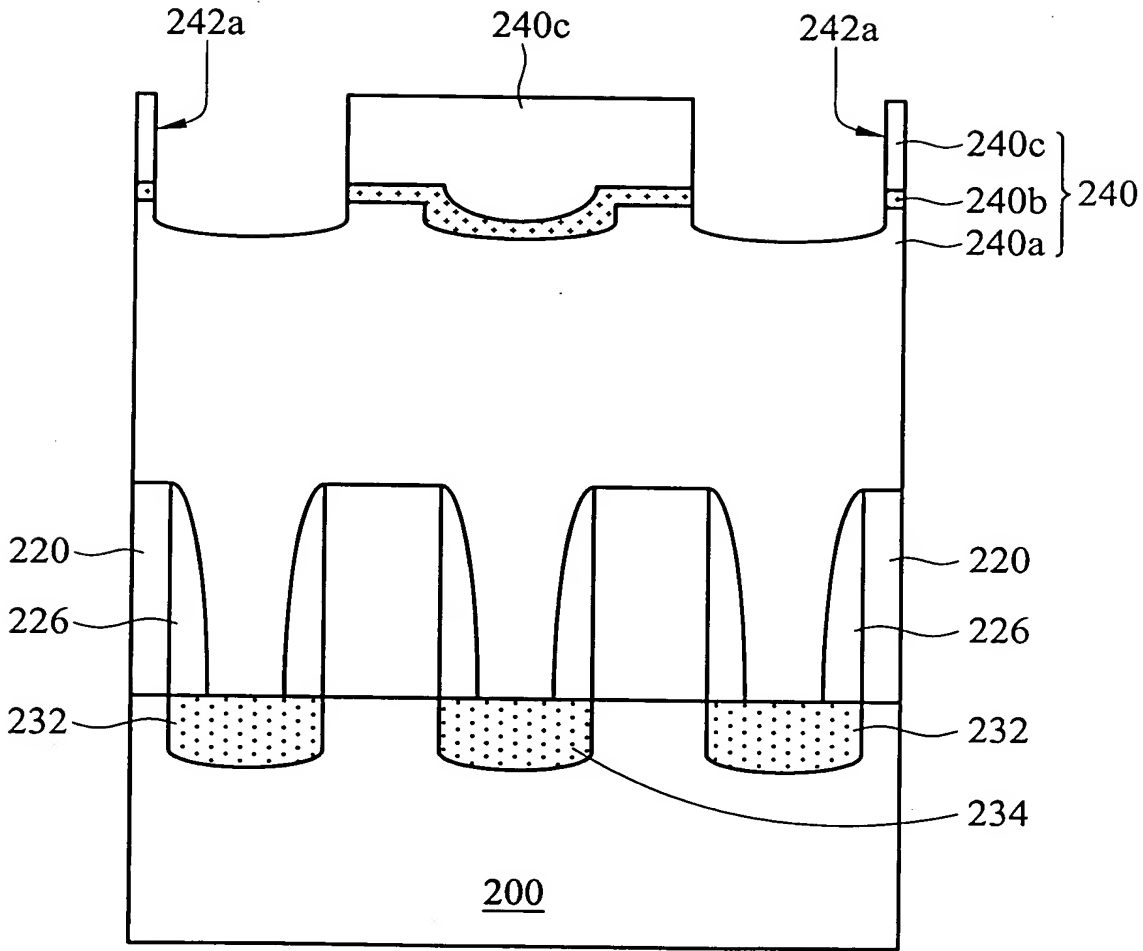


FIG. 6F

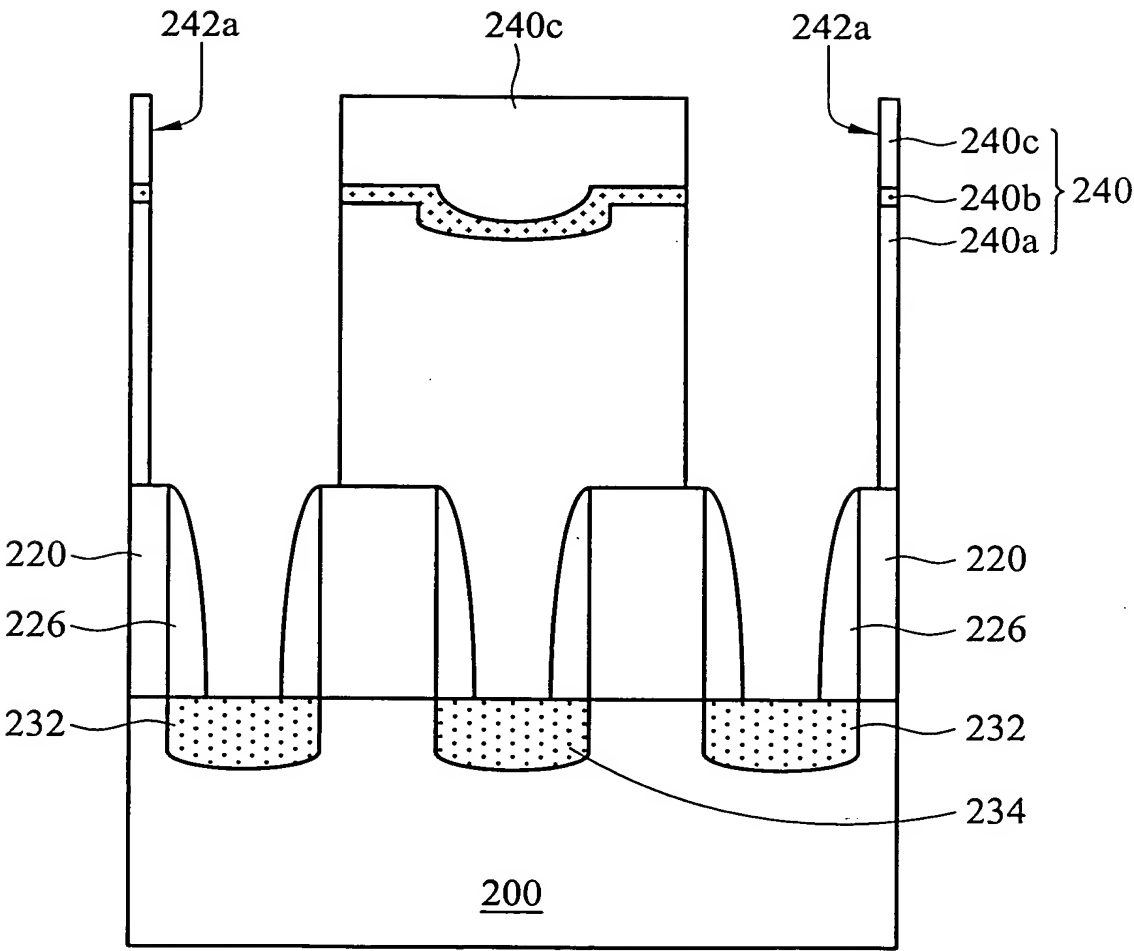


FIG. 6G

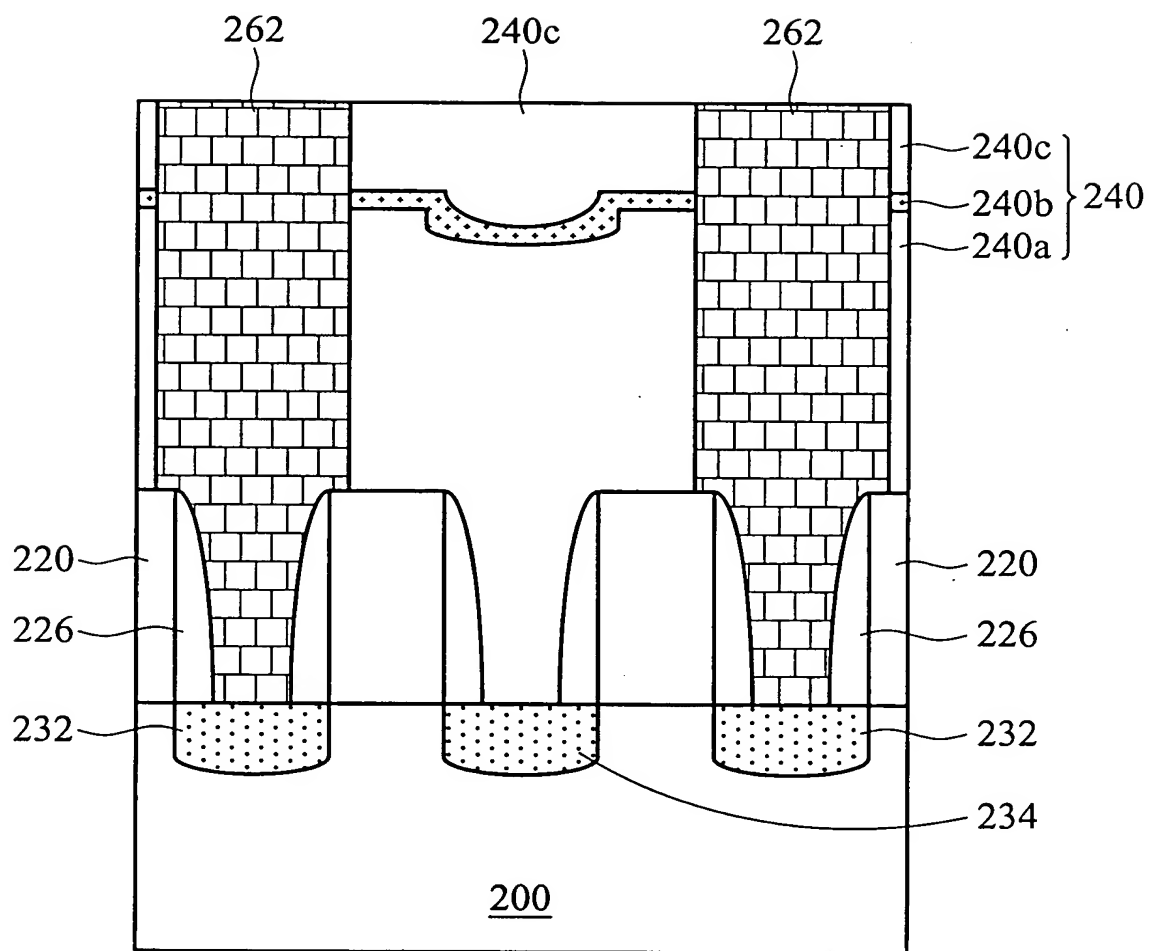


FIG. 6H